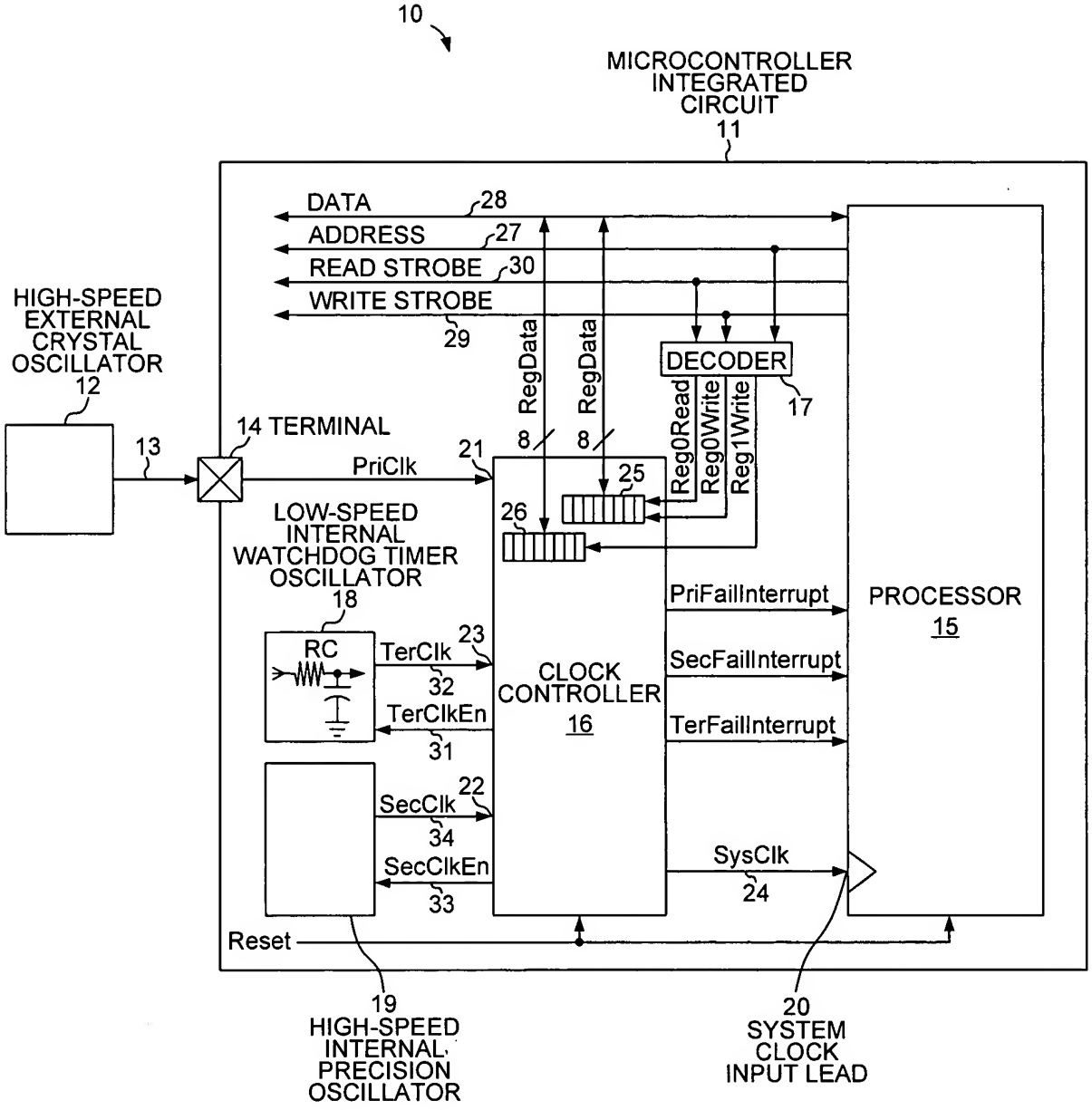
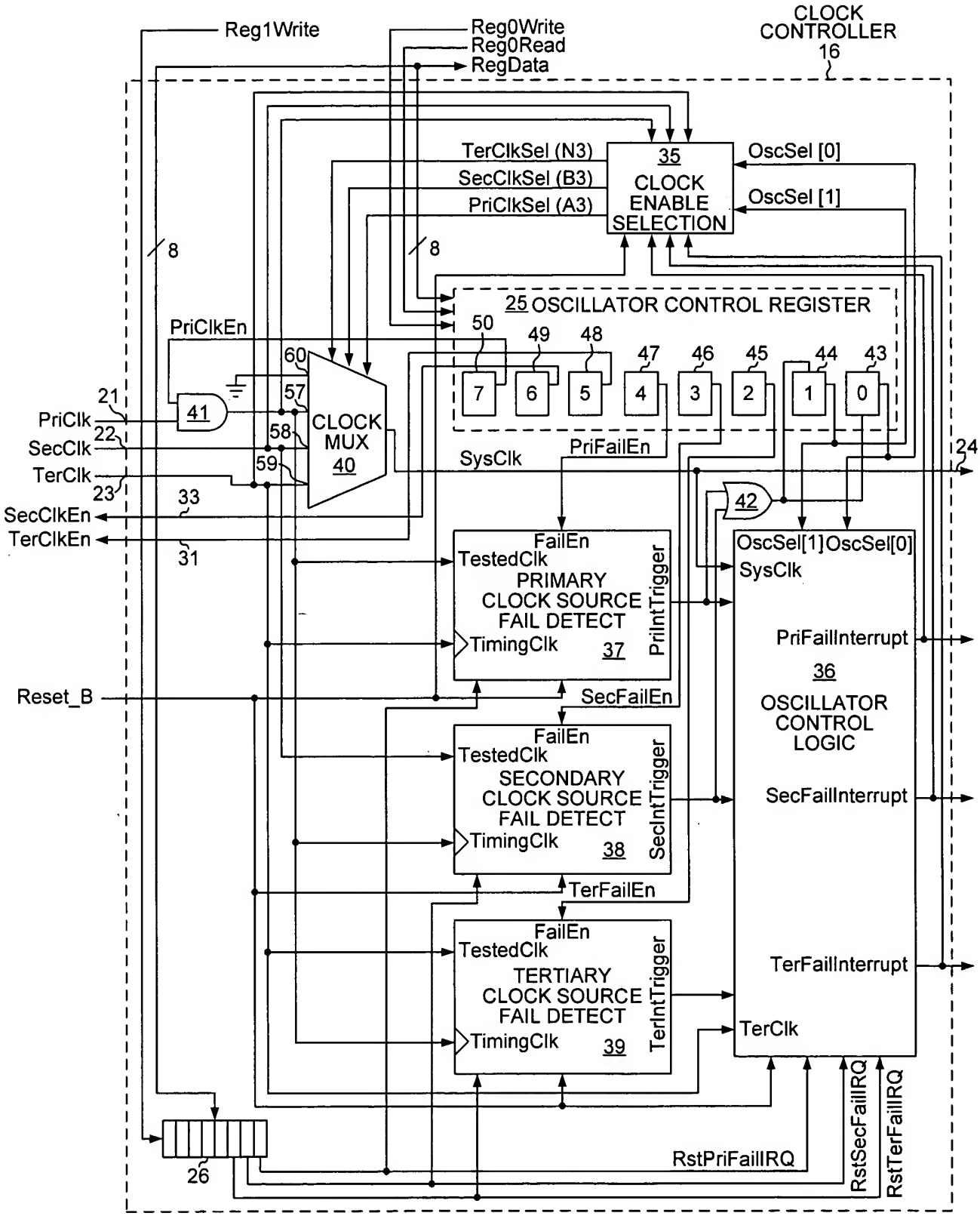
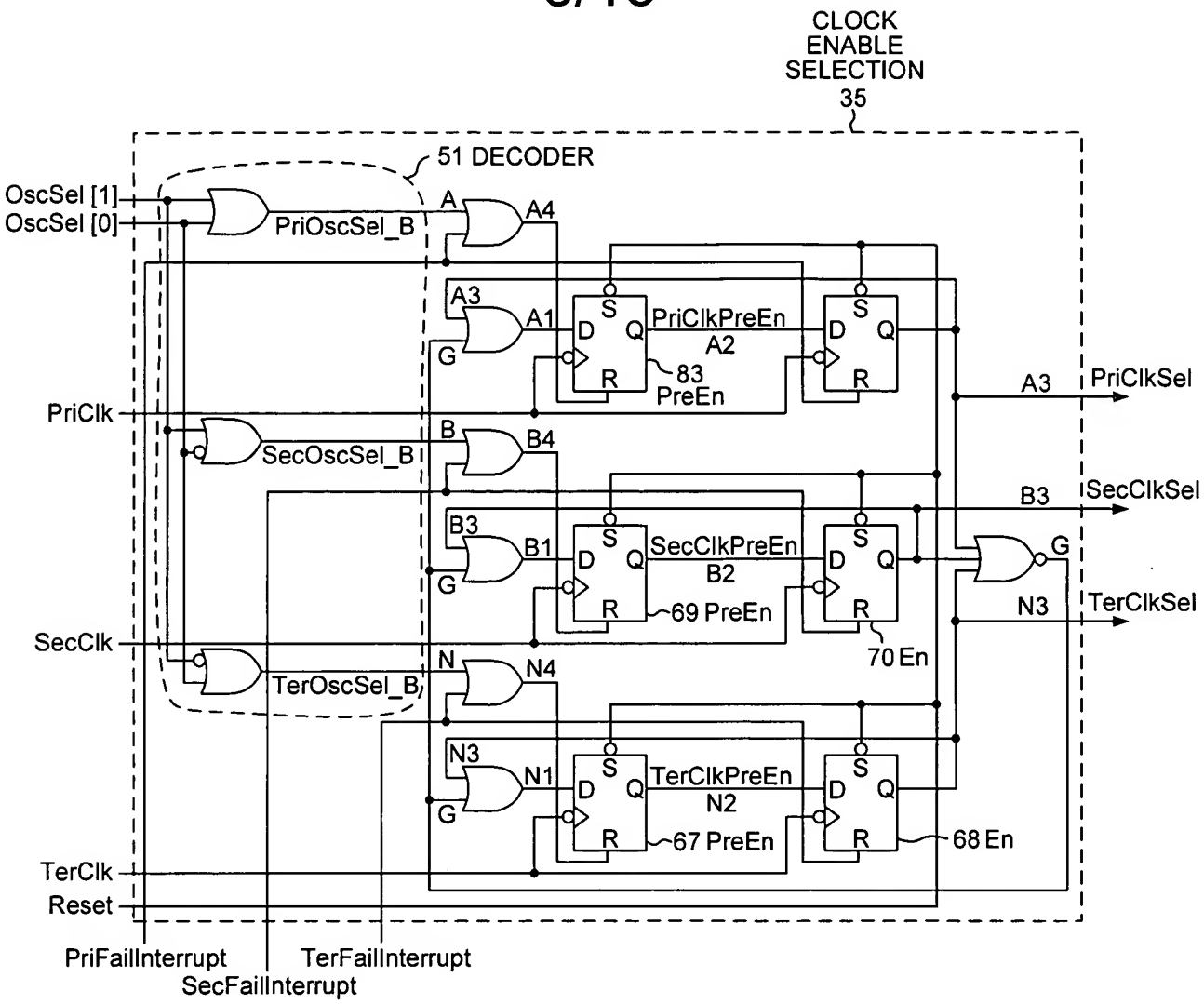

10
MICROCONTROLLER INTEGRATED CIRCUIT
11
DATA
28
ADDRESS
27
READ STROBE
30
WRITE STROBE
29
HIGH-SPEED EXTERNAL CRYSTAL OSCILLATOR
12
13
14 TERMINAL
PriClk
21
RegData
8
RegData
8
DECODER
17
Reg0Read
Reg0Write
Reg1Write
25
26
LOW-SPEED INTERNAL WATCHDOG TIMER OSCILLATOR
18
RC
TerClk
23
32
TerClkEn
31
SecClk
22
34
SecClkEn
33
CLOCK CONTROLLER
16
PriFailInterrupt
SecFailInterrupt
TerFailInterrupt
SysClk
24
PROCESSOR
15
Reset
19
HIGH-SPEED INTERNAL PRECISION OSCILLATOR
20
SYSTEM CLOCK INPUT LEAD

FIG. 1



CLOCK CONTROLLER

FIG. 2

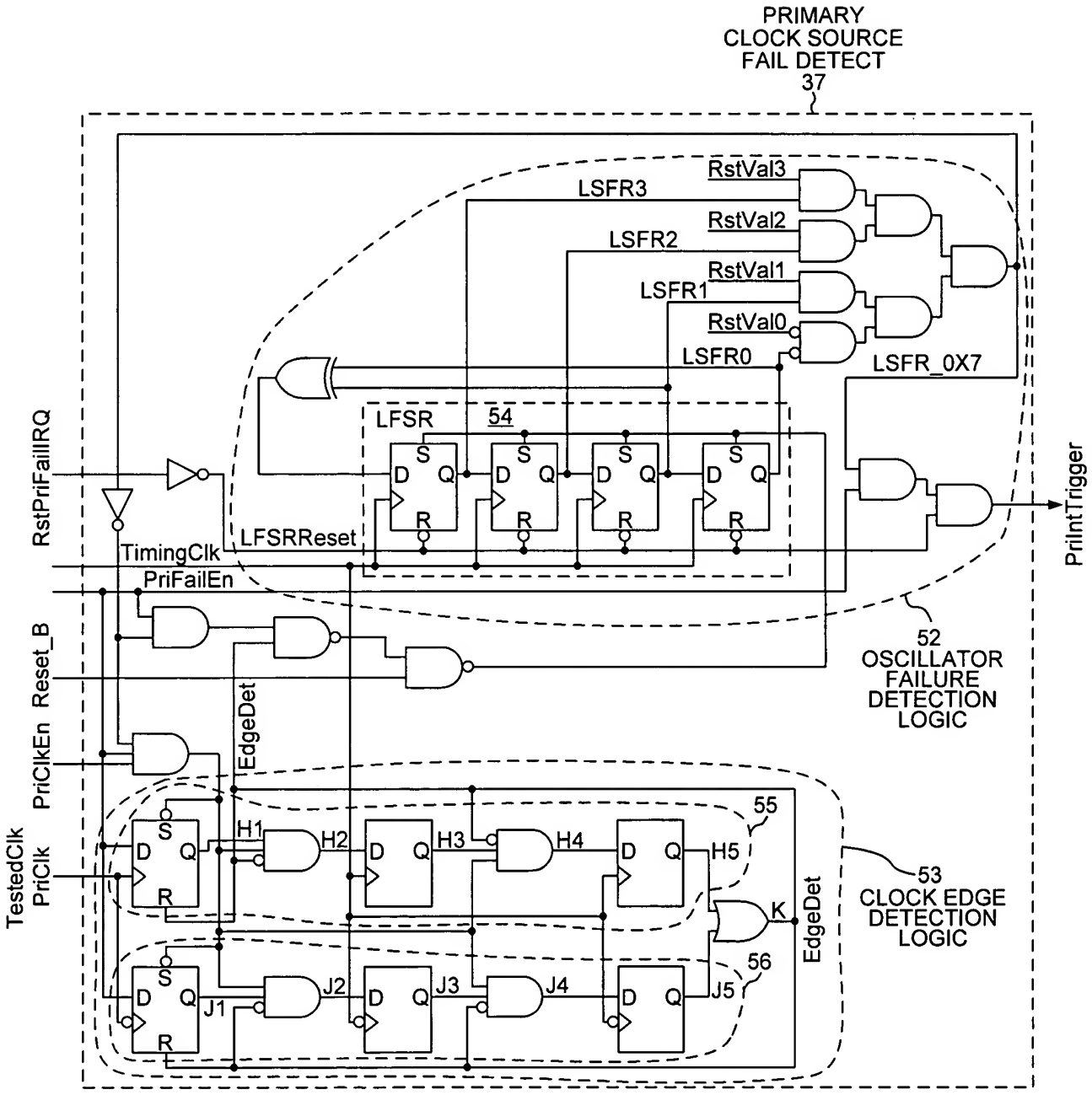


CLOCK ENABLE SELECTION

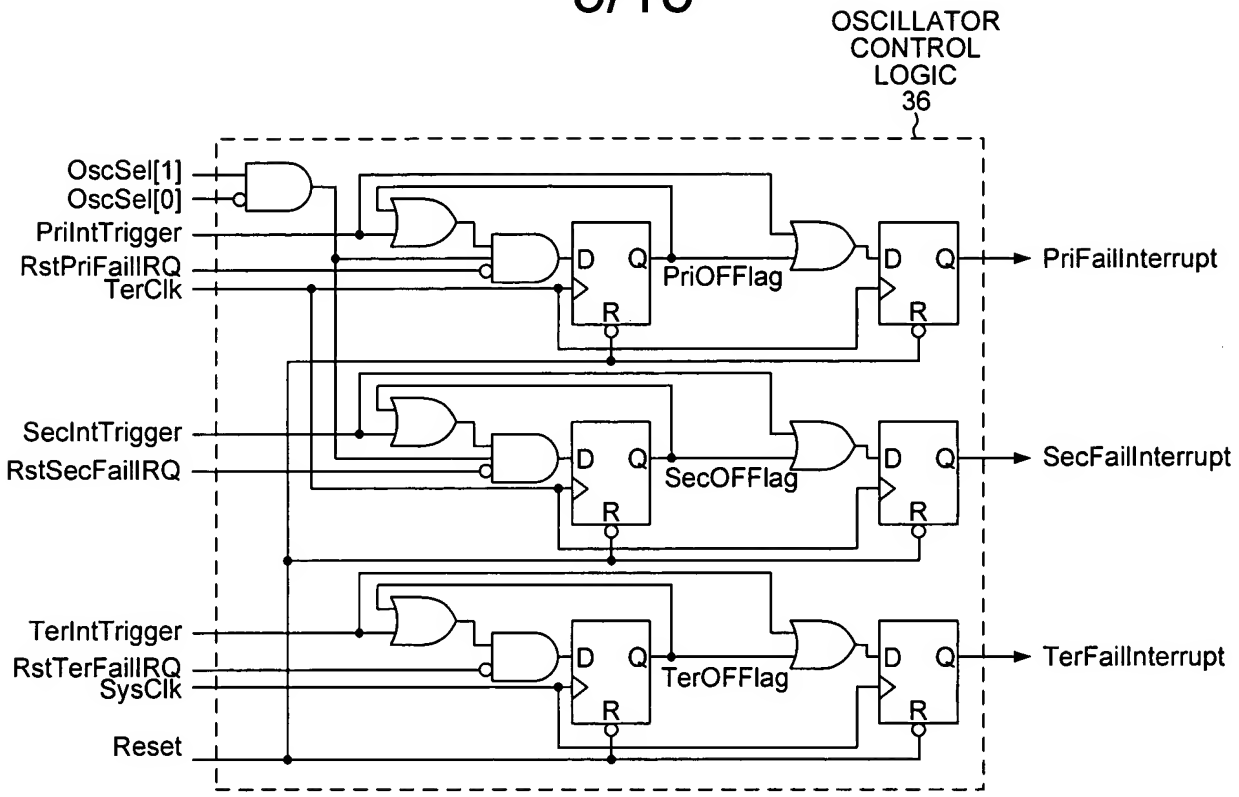
FIG. 3

OUTPUTS FROM CLOCK ENABLE SELECTION 35			INPUTS OF DECODER 51
PriClkSel A3	SecClkSel B3	TerClkSel N3	OscSel [1:0]
1	0	0	00
0	1	0	01
0	0	1	10
0	0	0	11

FIG. 7

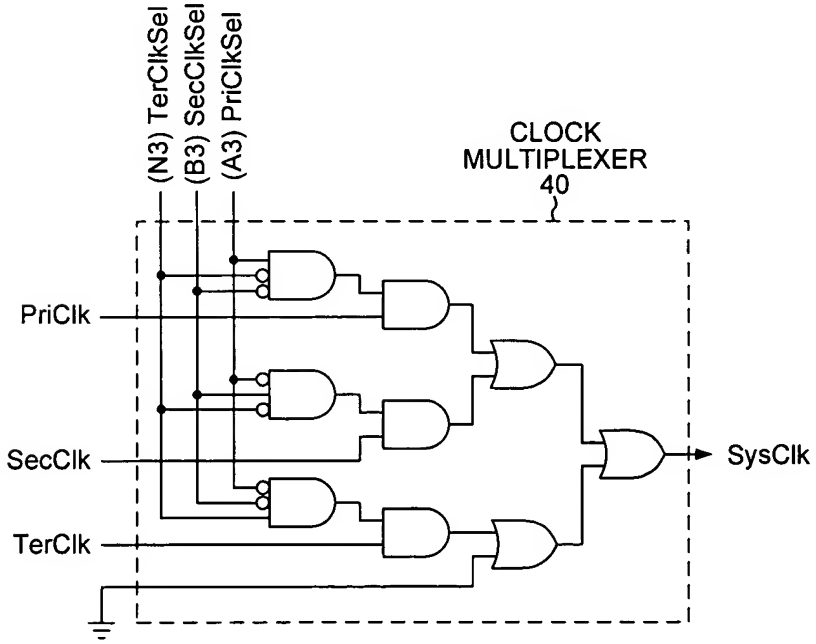


PRIMARY CLOCK
SOURCE FAIL DETECT
FIG. 4



OSCILLATOR CONTROL LOGIC

FIG. 5



CLOCK MULTIPLEXER

FIG. 6

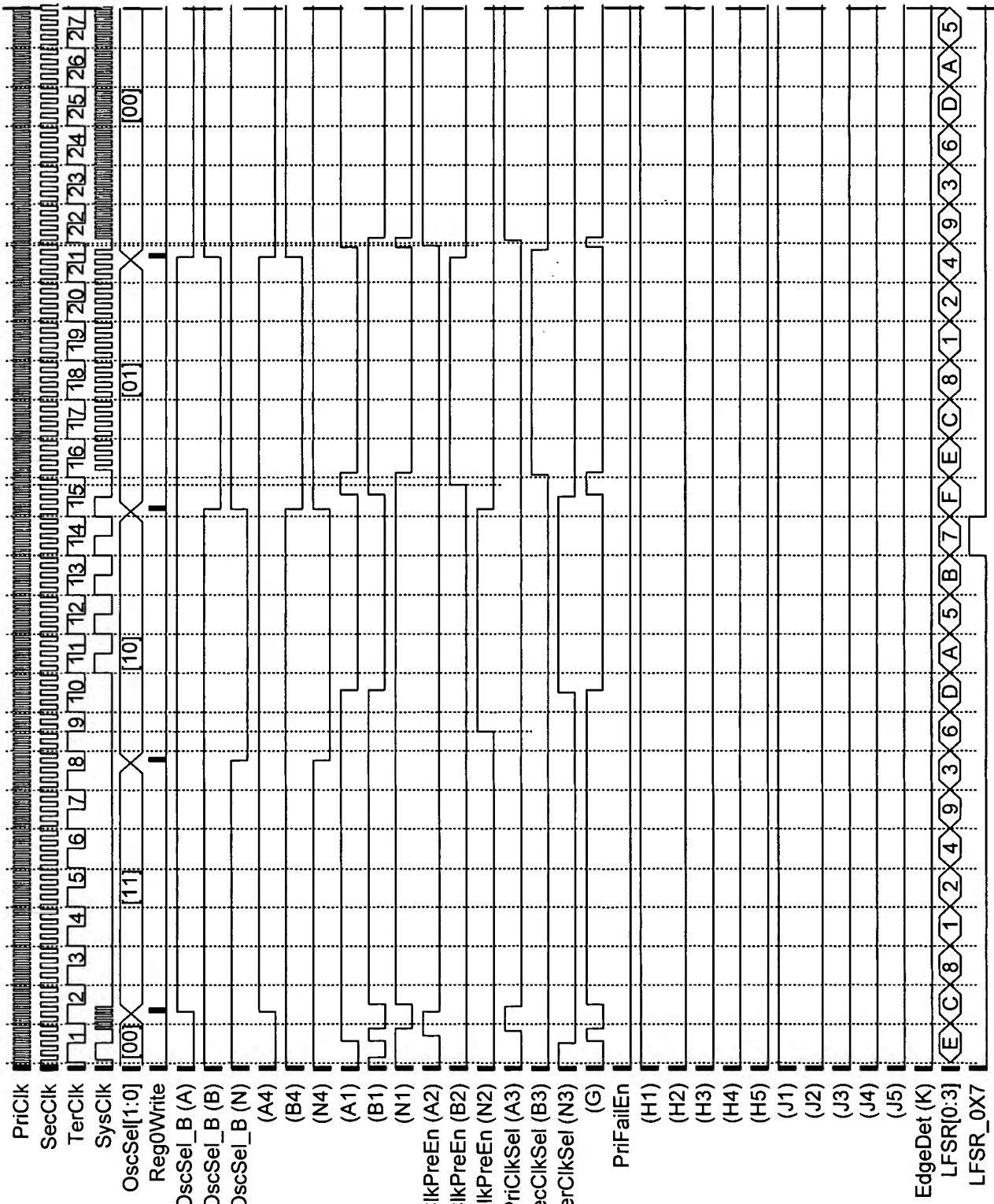


FIG. 8A

KEY TO FIG. 8

FIG. 8A	FIG. 8B	FIG. 8C

FIG. 8

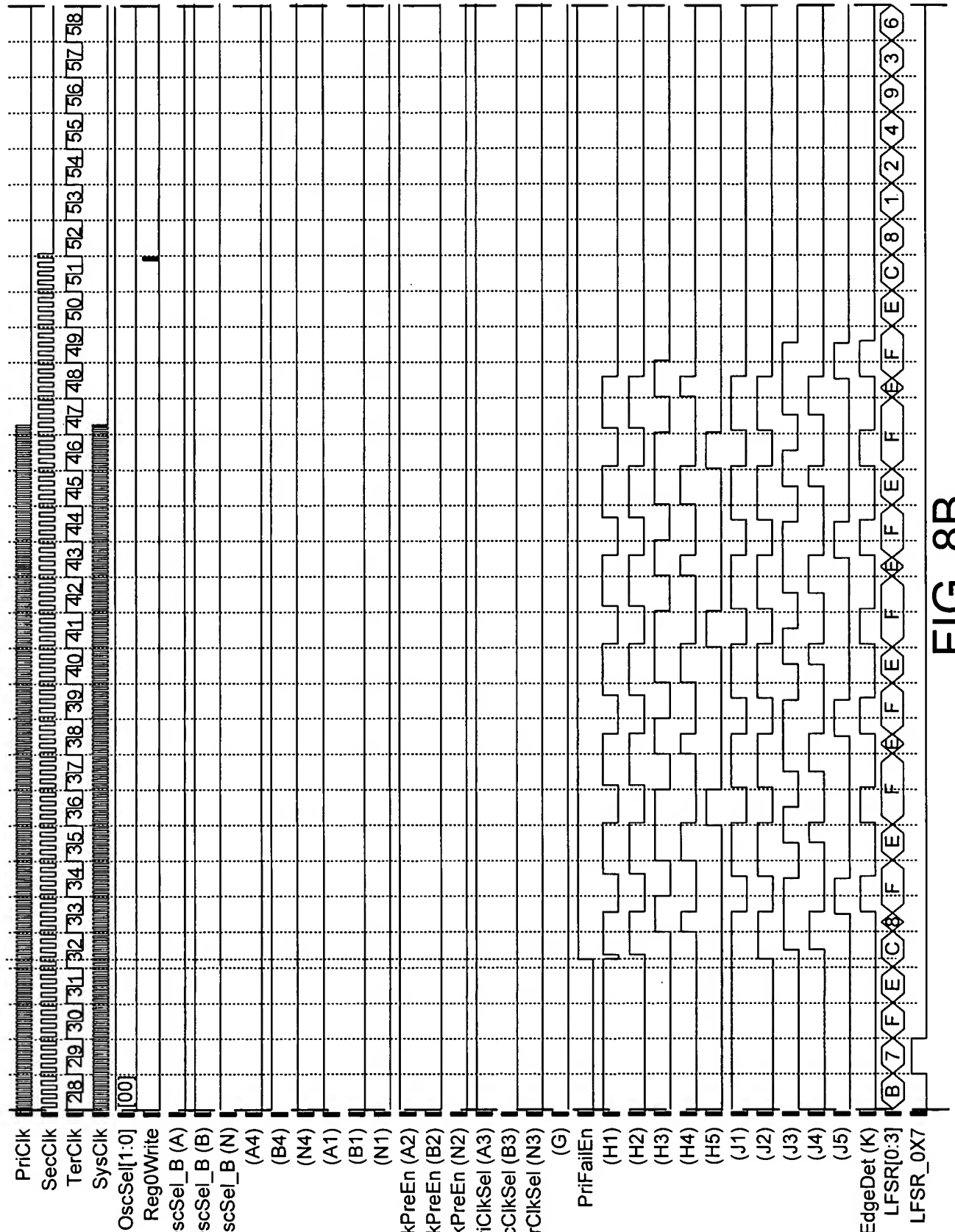

PriClk
SecClk
TerClk
SysClk
OscSel[1:0]
Reg0Write
PriOscSel_B (A)
SecOscSel_B (B)
TerOscSel_B (N)
(A4)
(B4)
(N4)
(A1)
(B1)
(N1)
PriClkPreEn (A2)
SecClkPreEn (B2)
TerClkPreEn (N2)
PriClkSel (A3)
SecClkSel (B3)
TerClkSel (N3)
(G)
PriFailEn
(H1)
(H2)
(H3)
(H4)
(H5)
(J1)
(J2)
(J3)
(J4)
(J5)
EdgeDet (K)
LFSR[0:3]
LFSR_0X7
28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58
00
B 7 F E C 8 F E F E F E F E F E F E F E F E C 8 1 2 4 9 3 6

FIG. 8B

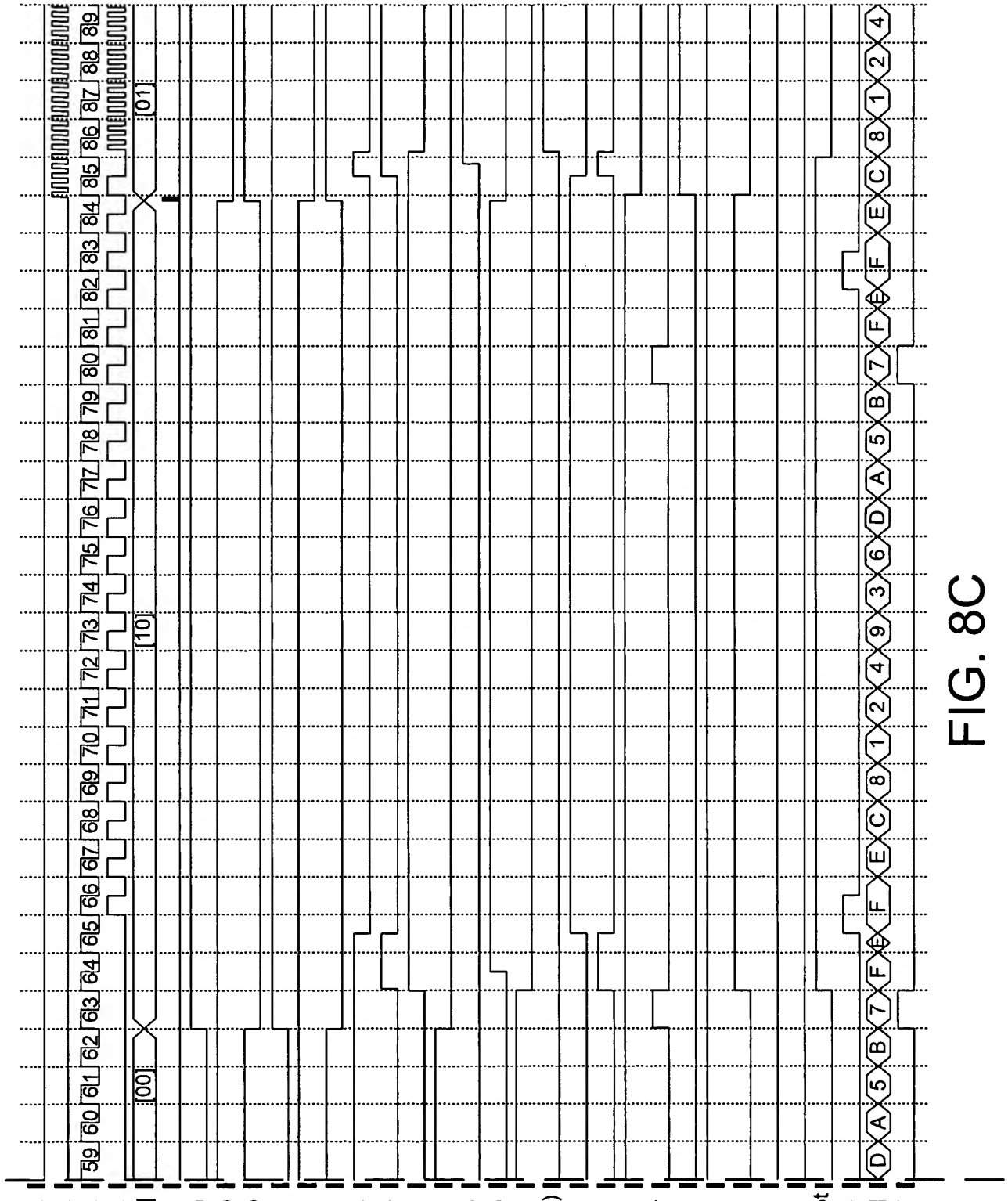
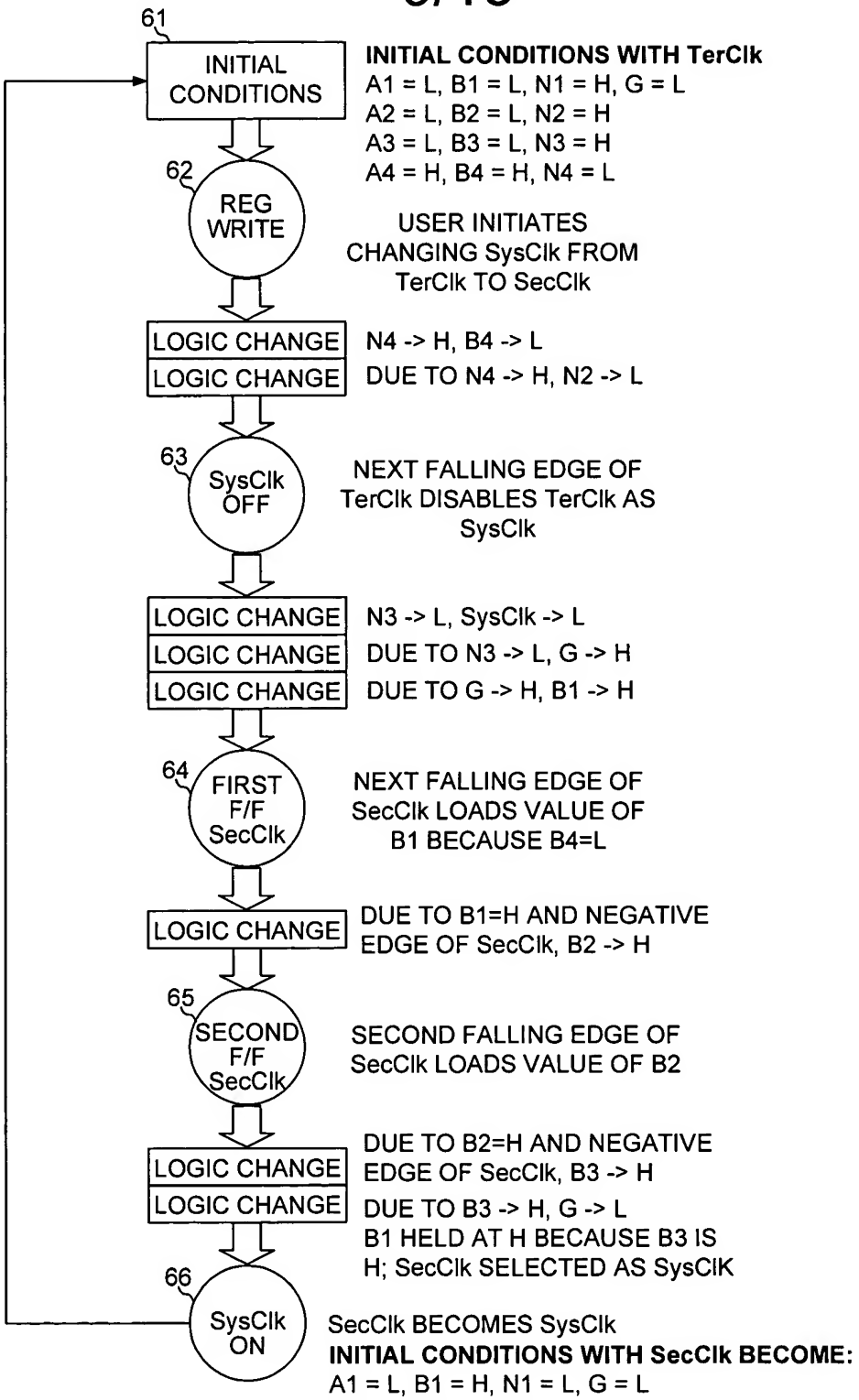

PriClk
SecClk
TerClk
SysClk
OscSel[1:0]
Reg0Write
PriOscSel_B (A)
SecOscSel_B (B)
TerOscSel_B (N)
(A4)
(B4)
(N4)
(A1)
(B1)
(N1)
PriClkPreEn (A2)
SecClkPreEn (B2)
TerClkPreEn (N2)
PriClkSel (A3)
SecClkSel (B3)
TerClkSel (N3)
(G)
PriFailEn
PriIntTrigger
RstPriFailIRQ
PriClkEn
PriOFFLag
SecOFFLag
TerOFFLag
PriFailInterrupt
EdgeDet (K)
LFSR[0:3]
LFSR_0X7
[00]
[10]
[01]

FIG. 8C



KEY FOR FIGURES 9 - 11

H	MEANS LOGIC HIGH
L	MEANS LOGIC LOW
->	MEANS CHANGES STATE
=	MEANS CURRENT STATE

FIG. 9

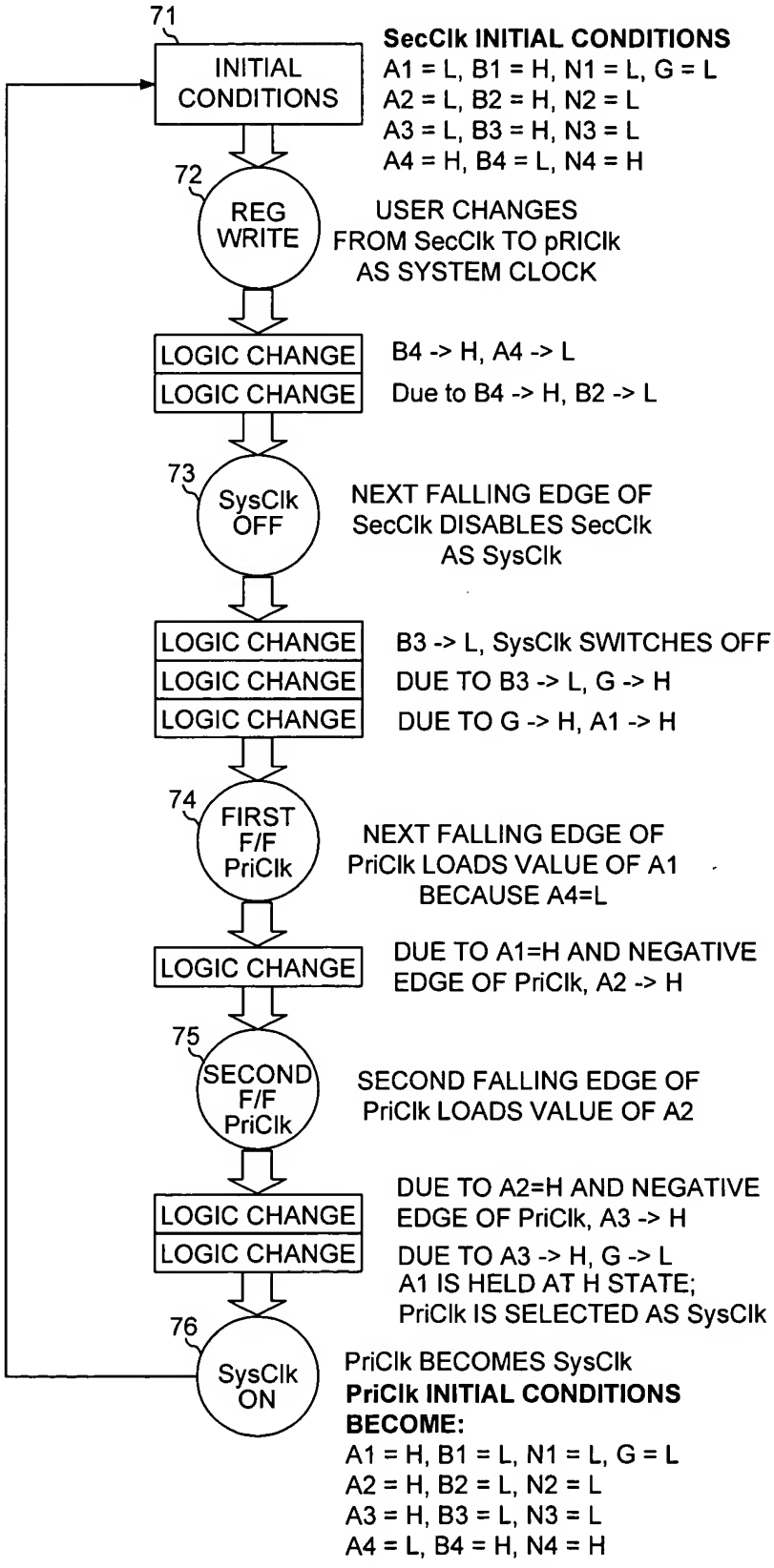

71
INITIAL CONDITIONS
SecClk INITIAL CONDITIONS
A1 = L, B1 = H, N1 = L, G = L
A2 = L, B2 = H, N2 = L
A3 = L, B3 = H, N3 = L
A4 = H, B4 = L, N4 = H
72
REG WRITE
USER CHANGES FROM SecClk TO pRIClk AS SYSTEM CLOCK
LOGIC CHANGE
B4 -> H, A4 -> L
LOGIC CHANGE
Due to B4 -> H, B2 -> L
73
SysClk OFF
NEXT FALLING EDGE OF SecClk DISABLES SecClk AS SysClk
LOGIC CHANGE
B3 -> L, SysClk SWITCHES OFF
LOGIC CHANGE
DUE TO B3 -> L, G -> H
LOGIC CHANGE
DUE TO G -> H, A1 -> H
74
FIRST F/F PriClk
NEXT FALLING EDGE OF PriClk LOADS VALUE OF A1 BECAUSE A4=L
LOGIC CHANGE
DUE TO A1=H AND NEGATIVE EDGE OF PriClk, A2 -> H
75
SECOND F/F PriClk
SECOND FALLING EDGE OF PriClk LOADS VALUE OF A2
LOGIC CHANGE
DUE TO A2=H AND NEGATIVE EDGE OF PriClk, A3 -> H
LOGIC CHANGE
DUE TO A3 -> H, G -> L
A1 IS HELD AT H STATE;
PriClk IS SELECTED AS SysClk
76
SysClk ON
PriClk BECOMES SysClk
PriClk INITIAL CONDITIONS BECOME:
A1 = H, B1 = L, N1 = L, G = L
A2 = H, B2 = L, N2 = L
A3 = H, B3 = L, N3 = L
A4 = L, B4 = H, N4 = H

FIG. 10

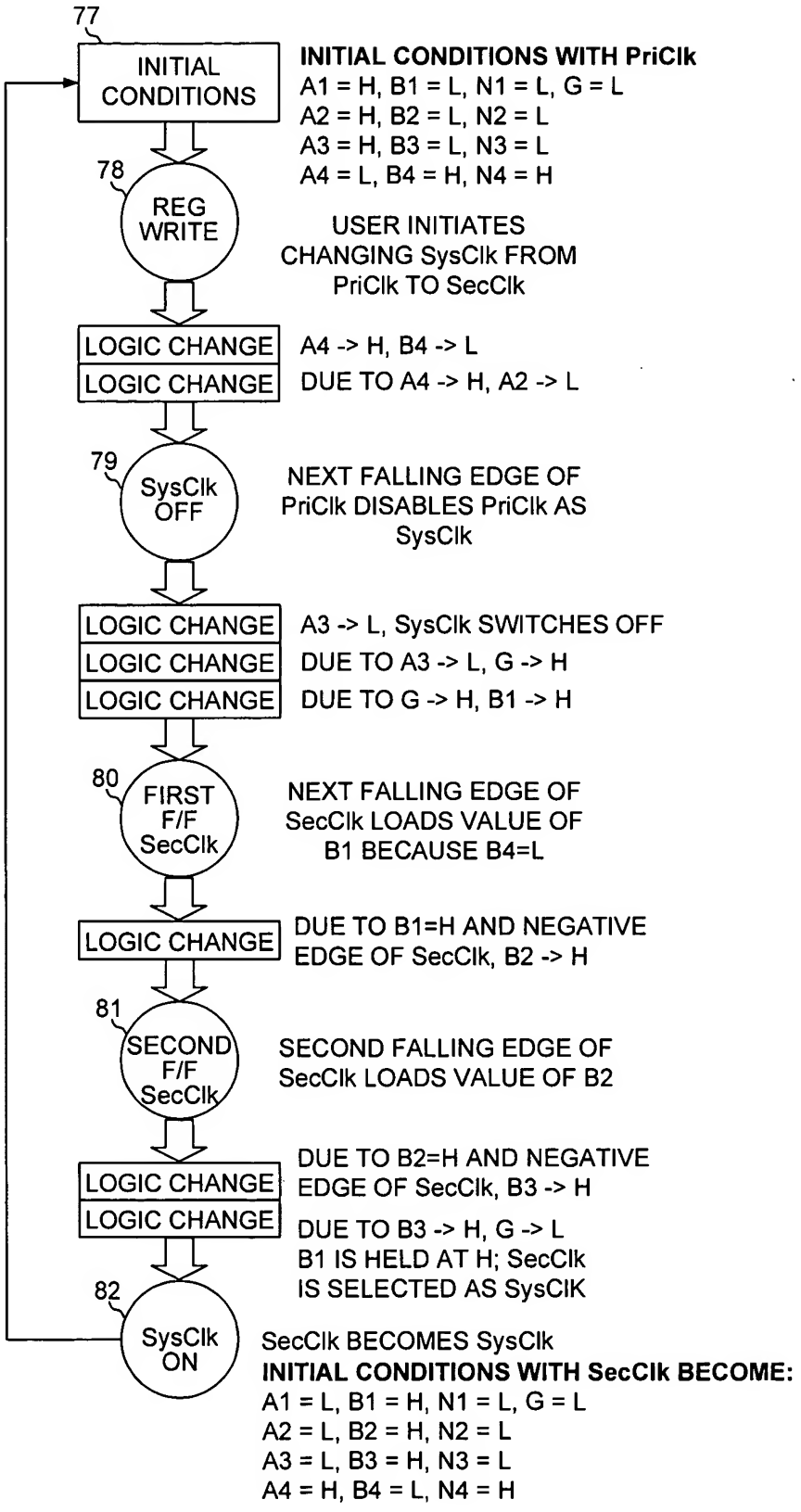
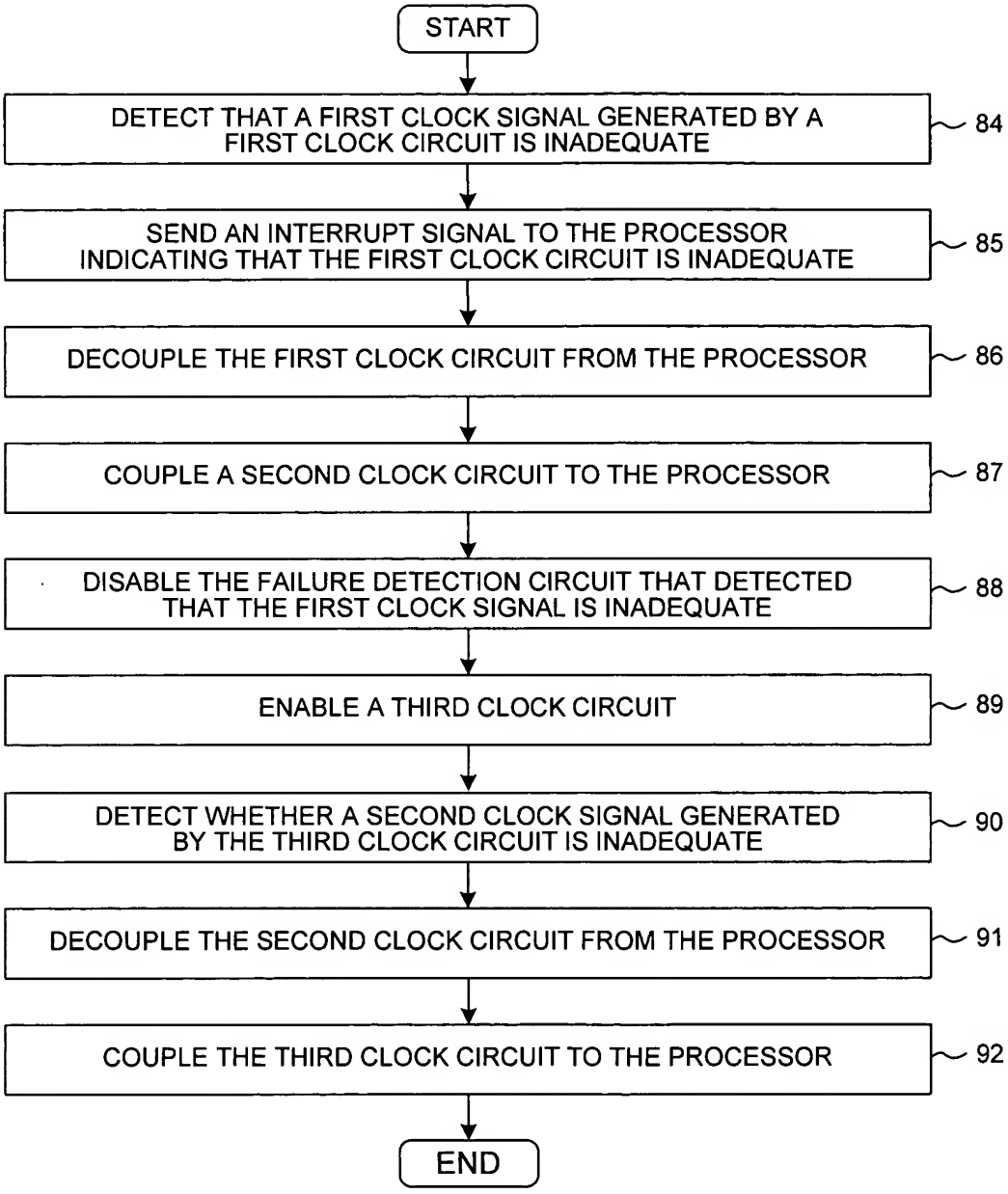

77
INITIAL CONDITIONS
INITIAL CONDITIONS WITH PriClk
A1 = H, B1 = L, N1 = L, G = L
A2 = H, B2 = L, N2 = L
A3 = H, B3 = L, N3 = L
A4 = L, B4 = H, N4 = H
78
REG WRITE
USER INITIATES CHANGING SysClk FROM PriClk TO SecClk
LOGIC CHANGE
LOGIC CHANGE
A4 -> H, B4 -> L
DUE TO A4 -> H, A2 -> L
79
SysClk OFF
NEXT FALLING EDGE OF PriClk DISABLES PriClk AS SysClk
LOGIC CHANGE
LOGIC CHANGE
LOGIC CHANGE
A3 -> L, SysClk SWITCHES OFF
DUE TO A3 -> L, G -> H
DUE TO G -> H, B1 -> H
80
FIRST F/F SecClk
NEXT FALLING EDGE OF SecClk LOADS VALUE OF B1 BECAUSE B4=L
LOGIC CHANGE
DUE TO B1=H AND NEGATIVE EDGE OF SecClk, B2 -> H
81
SECOND F/F SecClk
SECOND FALLING EDGE OF SecClk LOADS VALUE OF B2
LOGIC CHANGE
LOGIC CHANGE
DUE TO B2=H AND NEGATIVE EDGE OF SecClk, B3 -> H
DUE TO B3 -> H, G -> L
B1 IS HELD AT H; SecClk IS SELECTED AS SysClk
82
SysClk ON
SecClk BECOMES SysClk
INITIAL CONDITIONS WITH SecClk BECOME:
A1 = L, B1 = H, N1 = L, G = L
A2 = L, B2 = H, N2 = L
A3 = L, B3 = H, N3 = L
A4 = H, B4 = L, N4 = H

FIG. 11



SWITCHING FROM A FAILED CLOCK TO A NEW CLOCK

FIG. 12

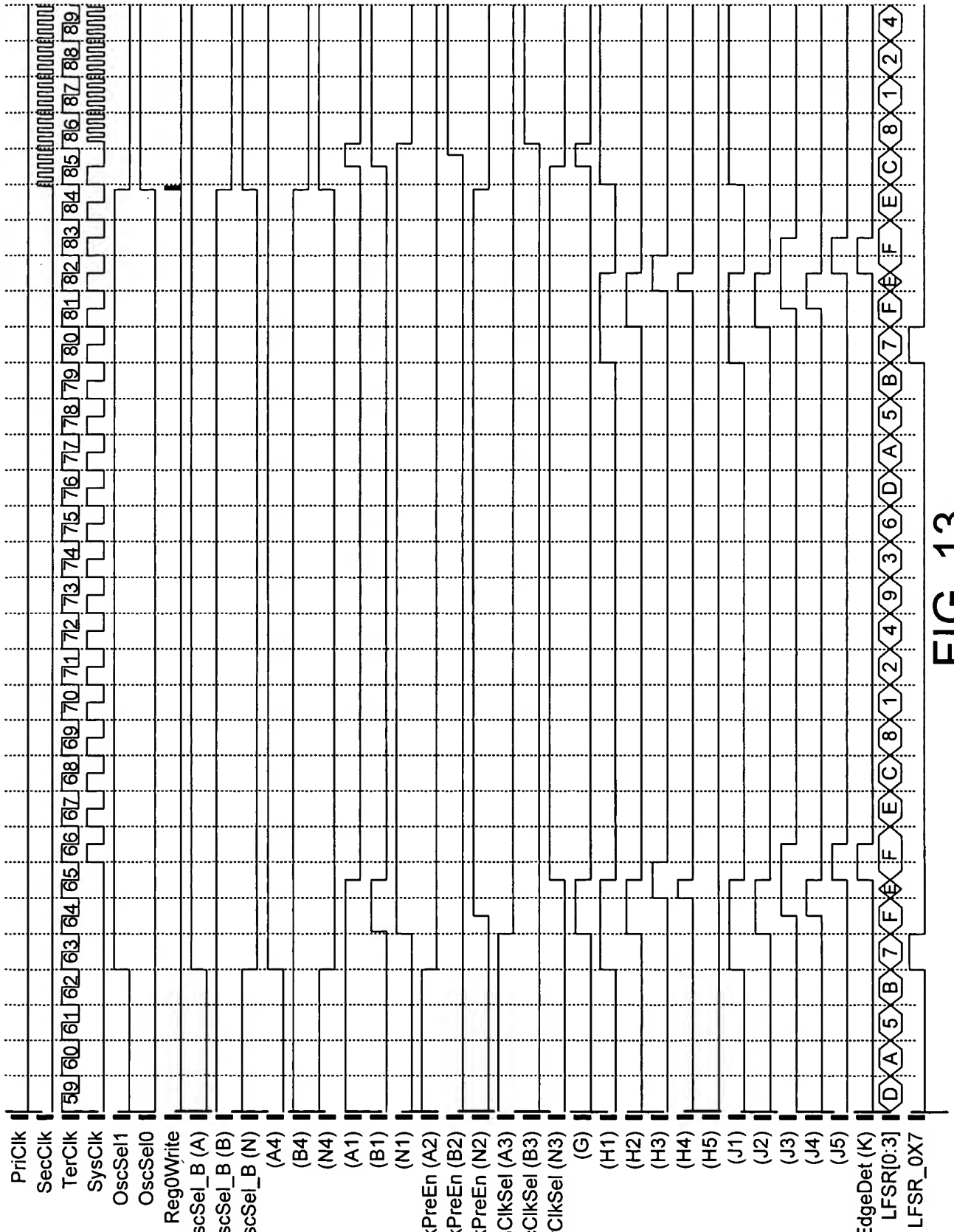

PriClk
SecClk
TerClk
SysClk
OscSel1
OscSel0
Reg0Write
PriOscSel_B (A)
SecOscSel_B (B)
TerOscSel_B (N)
(A4)
(B4)
(N4)
(A1)
(B1)
(N1)
PriClkPreEn (A2)
SecClkPreEn (B2)
TerClkPreEn (N2)
PriClkSel (A3)
SecClkSel (B3)
TerClkSel (N3)
(G)
(H1)
(H2)
(H3)
(H4)
(H5)
(J1)
(J2)
(J3)
(J4)
(J5)
EdgeDet (K)
LFSR[0:3]
LFSR_0X7

FIG. 13